Parametric and Functional Tests on SDRAM Video Memory

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LTG has faced the problem to perform a series of tests to up-screening (elevation of the level of quality / reliability) a lot of 4 Mbit SDRAM Video memories: the procedure involves the verification of the electrical characteristics critical (only those that we considered significant, or more subject to possible degradation) before and after each environmental test, in order to discard the components proved failures, but, more importantly, to measure the deviation of the electrical characteristics from the initial conditions, and/or when the environmental tests are satisfied.

After evaluating the opportunity to purchase or lease a “new generation ATE”, our technical staff, evaluating purely economic considerations, has decided to recondition our HP81810S system and to create "ad hoc" a special interface with LabVIEW software in order to measure the electrical parameters .

Fig.1 - Test System HP8180S (rack in preparation)

The HP81810S (see Fig. 1) consists of a series of rack-mounted equipment and a test head HP15425A with 84 pods. The rack contains the following equipment: HP4141B, Source / Monitor Unit (SMU) 4-channel DC parametric tests, Data Analyzer HP8182A for the capture of the pattern output from the DUT and related measures in AC. Pattern Generator HP8180A for parametric measurements in AC. An HP6624A multiple outputs power supply the power to the DUT and accessories. A customized card has a 10 Mips processor (Microchip 18F4620) joins the pattern generator HP8180A: these compose the whole Algorithmic Pattern Generator (APG) and is controlled by the USB-6221, and, finally, the GPIB -USB-HS interface connects HPIB bus from the inside of the rack to the external control computer.

The test program proceeds with the following steps:

a) contact, open, short, and leakage – test performed by HP4141B.
b) functional test – performed with the MATS++ and MARCH X algorithms by means of the APG card.
c) DC parametric – executed with the HP4141B and HP8182A using the MOVI algorithm.
d) AC parametric – performed by HP8180A with using MOVI algorithm.

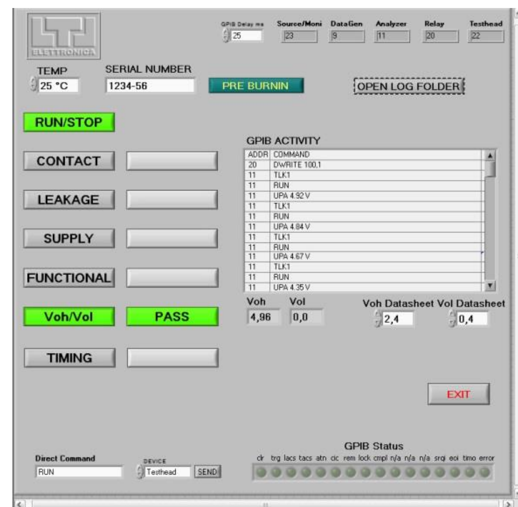

Fig.2 - Control Panel for managing the sequence of test

This sequence is clearly visible in the software control panel (see Fig. 2). Each rectangle indicates the execution of a specific test sequence. In addition, the steps can be performed completely automatically in the order indicated: the green light indicates the success of the test, the red light “test failed”. If it is necessary, it is possible to repeat manually each test.

The contact test (a) is performed by activating the protection diodes inside the device: sending on each pin a current of about 100 µA the junction voltage is measured. Later, after adjusting device in high impedance, the insulation of each pin (leakage current) is measured: These are performed by one of the HP4141B SMU. For the implementation of the functional test (b) we chose a MATS++ algorithm (Modified Algorithmic Test Sequence), Nair, 1979 (complexity 6n).

Other types of test algorithms (MSCAN, GALPAT, WALPAT) would have required a much greater number of iterations as nonlinear.

The causes of failure (fault occurrences) in a memory were modeled according to the following schemes::

- SAF (Stuck-at-fault) – the logical value of a memory cell does not change state: remains at 0 or 1.
- TF (Transition Faults) – The memory cell that does not perform a transition from 0 →1 or 1→ 0
- CF (Coupling Faults) – the memory cell changes its value when it is written to a neighbor cell
- AF (Address decoding fault) – lack of access to a group of cells, the memory cells accessed by multiple addresses, activated cells from multiple addresses simultaneously.

The MATS + + algorithm consists of the following steps:

1) write 0 in all cells,
2) read 0 by increasing the addresses, and then write 1,
3) read 1 by increasing the addresses, then write 0 and read 0 on the same memory location.

The algorithm detects exactly the errors due to SAF, AF, TF, and all possible occurrences of CF, if you adopt the variant MARCH X..

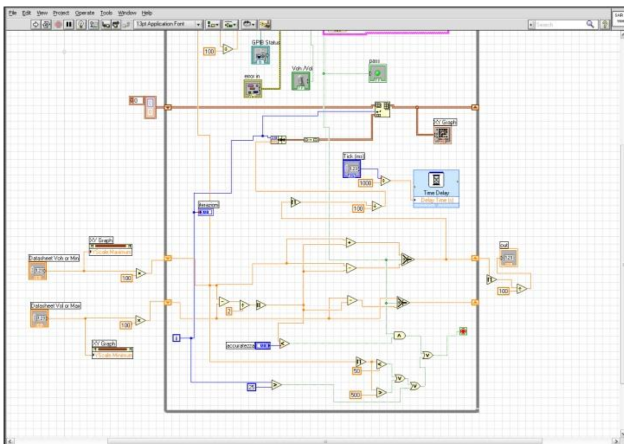

Fig.3 - Successive approximation algorithm for the measurement of V_{ol} and V_{oh}

We have developed another interesting algorithm in order to measure the voltages V_{ol} and V_{oh} of the device (see Fig. 3) , using the characteristics from the Data Analyzer HP8182A : The apparatus allows to program two voltage thresholds. The algorithm (SAR type) starts from the values of specific datasheets and, after applying a standard TTL load, checks for the presence of the pattern of output data (using a variant of the MOVI algorithm).

The next step is to change the value of the threshold voltage by means of successive approximations and the occurrence of an error condition , the last set threshold value indicates (within a tolerance margin settable) threshold output voltage.

Finally, the parametric measurements in AC adopted new algorithm MOVI: writing two different values in two opposite 2, based on a shift of the signals RAS, compared with the address CAS bus, is possible to test the access time, the Address Setup and Address Hold . For these measurements it is used the pattern generator HP8180A, which has the capability to vary the output signals (pattern) with a resolution of 100 ps.

Bibliography

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